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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/689,187	10/20/2003	N. Johan Knall	MA-002-1-I-a	2700
7590	01/21/2005		EXAMINER	
MATRIX SEMICONDUCTOR 3230 Scott Blvd Santa Clara, CA 95054				DOLAN, JENNIFER M
		ART UNIT		PAPER NUMBER
		2813		

DATE MAILED: 01/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H-1

Office Action Summary	Application No.	Applicant(s)	
	10/689,187	KNALL ET AL.	
	Examiner	Art Unit	
	Jennifer M. Dolan	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on _____.
- 2a) This action is **FINAL**. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1 and 2 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1 and 2 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 20 October 2003 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____. |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____. | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____. |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-2 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 4,881,114 to Mohsen et al. in view of U.S. Patent No. 5,835,396 to Zhang.

Mohsen discloses a memory array (figures 6, 7) disposed above a substrate (10), the array comprising a plurality of memory cells (figures 1, 2), each cell comprising a silicon nitride antifuse (14; column 4, lines 21-25), the array further comprising p+n- diodes or p-n+ diodes (column 3, lines 45-55; “moderately doped” layer 12 and “heavily doped” layer 16 form diode).

Mohsen fails to disclose that the memory array is a three dimensional multi-level array.

Zhang discloses three dimensional multi-level memory arrays having units substantially similar to that of Mohsen (figures 1, 13; column 2, lines 20-50; column 5, lines 45-50; column 6, lines 1-10; 55-60).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the memory cell array of Mohsen, such that it is formed in a three dimensional, multi-level array, as suggested by Zhang. The rationale is as follows: A person having ordinary skill in the art would have been motivated to use a three dimensional array,

because doing so allows for an increase in memory density of the structure (Zhang, column 1, lines 60-67; column 2, lines 22-48).

3. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang in view of U.S. Patent No. 5,866,938 to Takagi et al.

Zhang discloses a three-dimensional multi-level memory array (figures 1, 13) disposed above a substrate (10), the array comprising a plurality of cells, each cell comprising an antifuse (column 5, line 45 – column 6, line 16).

Zhang fails to disclose that the antifuse is silicon nitride.

Takagi discloses that for a memory cell, silicon nitride is a preferred antifuse material (column 6, lines 1-35).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the antifuse layer of Zhang, such that it is silicon nitride, as taught by Takagi. The rationale is as follows: A person having ordinary skill in the art would have been motivated to use silicon nitride, because Takagi shows that it has high resistivity and a highly selectable breakdown voltage, thus allowing for a stable anti-fuse layer (see Takagi, column 2, lines 1-15; column 6, lines 1-35).

4. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang in view of Takagi et al. as applied to claim 1 above, and further in view of U.S. Patent No. 5,714,795 to Ohmi et al.

Zhang discloses that the array comprises p-n diodes (column 6, lines 50-62), but fails to specify the doping of the diode layers.

Ohmi discloses an antifuse memory cell having p-n+ diodes (69,70; column 14, lines 40-50).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to specify that the pn junction of Zhang as modified by Takagi is doped to be a p-n+ junction, as suggested by Ohmi. The rationale is as follows: A person having ordinary skill in the art would have been motivated to use a p-n+ junction, because such junctions decrease the reverse leakage currents through the memory cells and allow for an improved single-directional application of current through the cell, as is appreciated by one skilled in the art (also see Ohmi, column 3, lines 40-50).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 6,034,882 to Johnson et al. teaches a three dimensional array of memory cells using diodes.

U.S. Patent No. 6,291,836 to Kramer et al. discloses stacking memory elements using planarization intermediate layers in order to form a three dimensional array.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (571) 272-1690. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Dolan
Examiner
Art Unit 2813

jmd

Craig A. Thompson
CRAIG A. THOMPSON
PRIMARY EXAMINER